CLAIMS:

1. A method for determining filter coefficients for a digital filter, more particularly for the UMTS (Universal Mobile Telecommunication System), in which the filter coefficients are predetermined and modified in a filter design program, characterized in that the predetermined filter coefficients (b_v) are divided by a same scaling factor (s), in that the scaled filter coefficients ($ß_v$) are quantized by this, in that only a certain maximum number (n) of "1" bits are used counted from the most significant bit onwards and in that the quantization error of the quantized filter coefficient is determined relative to the predetermined filter coefficient and by repeated modification of the scaling factor (s) the respective scaling factor (s_0) is set in which the quantization error is minimal, and in that the filter coefficients ($ß_v$) having the minimal error are implemented in the filter.

2. A method as claimed in claim 1, characterized in that the number (n) is four or three or two.

3. A method as claimed in claim 1 or 2, characterized in that if again a "1" bit follows the last "1" bit, a rounding is effected from the last bit onwards.

4. A digital filter, more particularly for UMTS, in which the digital filter coefficients are processed with the signal, characterized in that the binary filter coefficients ($ß_v$) are scaled by a scaling factor (s_0) and in that the filter coefficients ($ß_v$) are quantized so that they do not exceed a certain number (n) of "1" bits from the most significant bit onwards, in that adder stages ADD(3) are provided which process the scaled and quantized filter coefficients ($ß_4$) with the signal.

5. A digital filter as claimed in claim 1, characterized in that the final stage (4) is provided which processes the output signal by a factor (s_0) reciprocal to the scaling factor.

6. A digital filter as claimed in claim 4, characterized in that each adder stage (3) comprises n-1 adders (9, 10, 11) and n squaring multipliers (5, 6, 7, 8).

7. A digital filter as claimed in claim 4 or 5, characterized in that in the adder stages (3) the number n of the squaring multipliers (5, 6, 7, 8) is different and the number of adders (9, 10, 11) is accordingly different.

8. A digital filter as claimed in claim 7, characterized in that individual adder stages (3) have only a single squaring multiplier.

9. A digital filter as claimed in one of the preceding claims, characterized in that the squaring multiplier (5, 6, 7, 8) is formed by connections of its inputs and outputs.

10. A digital filter as claimed in one of the preceding claims, characterized in that the adder stage (3) comprises a programmable selector (12) which in accordance with its programming connects the squaring multiplier (5, 6, 7, 8) with the adders (9, 11).